



Synchronous State-Machine Design

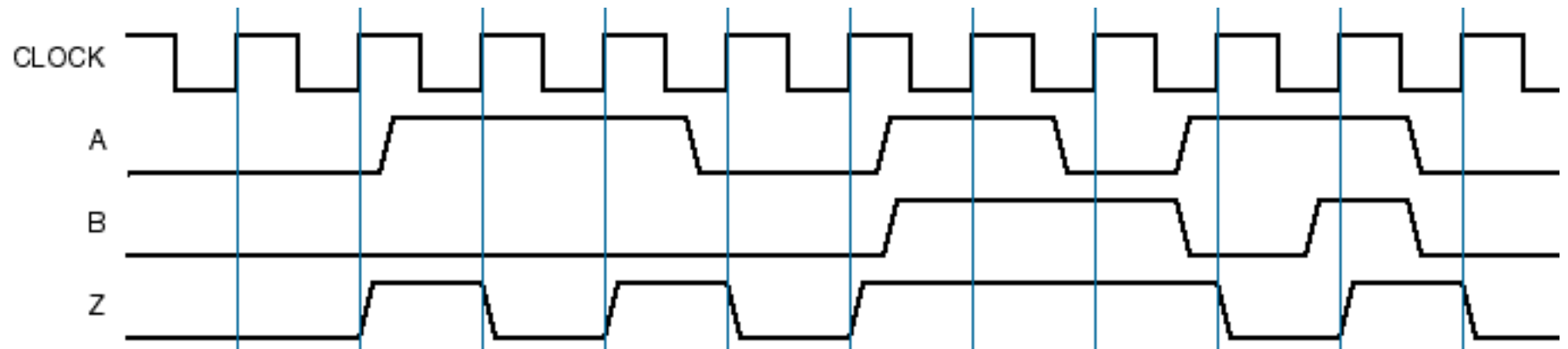
Synchronous State Machine Design Steps

1. Construct state/output table or state diagram.
2. Minimize number of states.
3. State assignment – binary code for each state.
4. Create transition/output table – decide how to handle unused states.
5. Select flip-flop type, i.e., D, T or J-K.
6. Construct excitation table.
7. Derive excitation & output equations.
8. Realize logic network with discrete gates & flip-flops or with programmable logic device.

State Table Design Example

- State machine with two inputs, A and B, and one output Z.
- $Z = 1$ if:
 - A has been the same for two consecutive clock cycles.
 - B has been 1 since the last time the first condition was true.
- Otherwise, $Z = 0$.

Timing Diagram



State Table Generation

(a)

Meaning	S	AB				Z
		00	01	11	10	
Initial state	INIT					0
...	...					
...	...					
...	...					

S*

(b)

Meaning	S	AB				Z
		00	01	11	10	
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0					0
Got a 1 on A	A1					0

S*

(c)

Meaning	S	AB				Z
		00	01	11	10	
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK	OK	A1	A1	0
Got a 1 on A	A1					0
Got two equal A inputs	OK					1

S*

(d)

Meaning	S	AB				Z
		00	01	11	10	
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK	OK	A1	A1	0
Got a 1 on A	A1	A0	A0	OK	OK	0
Got two equal A inputs	OK					1

S*

State Table Generation – Cont.

(a)

Meaning	S	AB				Z
		00	01	11	10	
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK	OK	A1	A1	0
Got a 1 on A	A1	A0	A0	OK	OK	0
Got two equal A inputs	OK	?	OK	OK	?	1

S*

(b)

Meaning	S	AB				Z
		00	01	11	10	
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK0	OK0	A1	A1	0
Got a 1 on A	A1	A0	A0	OK1	OK1	0
Two equal, A=0 last	OK0					1
Two equal, A=1 last	OK1					1

S*

(c)

Meaning	S	AB				Z
		00	01	11	10	
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK0	OK0	A1	A1	0
Got a 1 on A	A1	A0	A0	OK1	OK1	0
Two equal, A=0 last	OK0	OK0	OK0	OK1	A1	1
Two equal, A=1 last	OK1					1

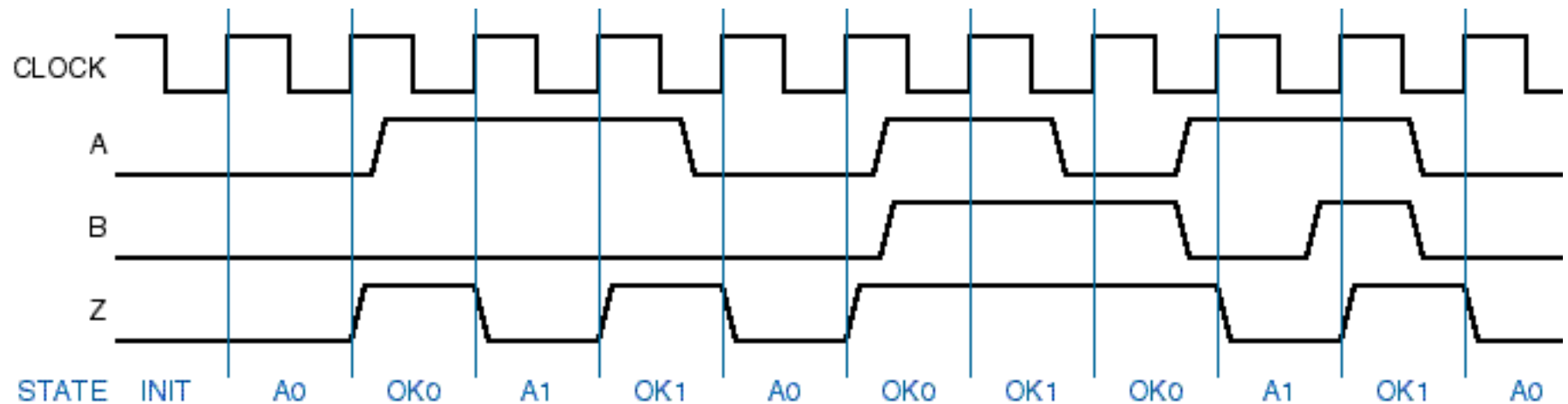
S*

(d)

Meaning	S	AB				Z
		00	01	11	10	
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK0	OK0	A1	A1	0
Got a 1 on A	A1	A0	A0	OK1	OK1	0
Two equal, A=0 last	OK0	OK0	OK0	OK1	A1	1
Two equal, A=1 last	OK1	A0	OK0	OK1	OK1	1

S*

Timing Diagram with States

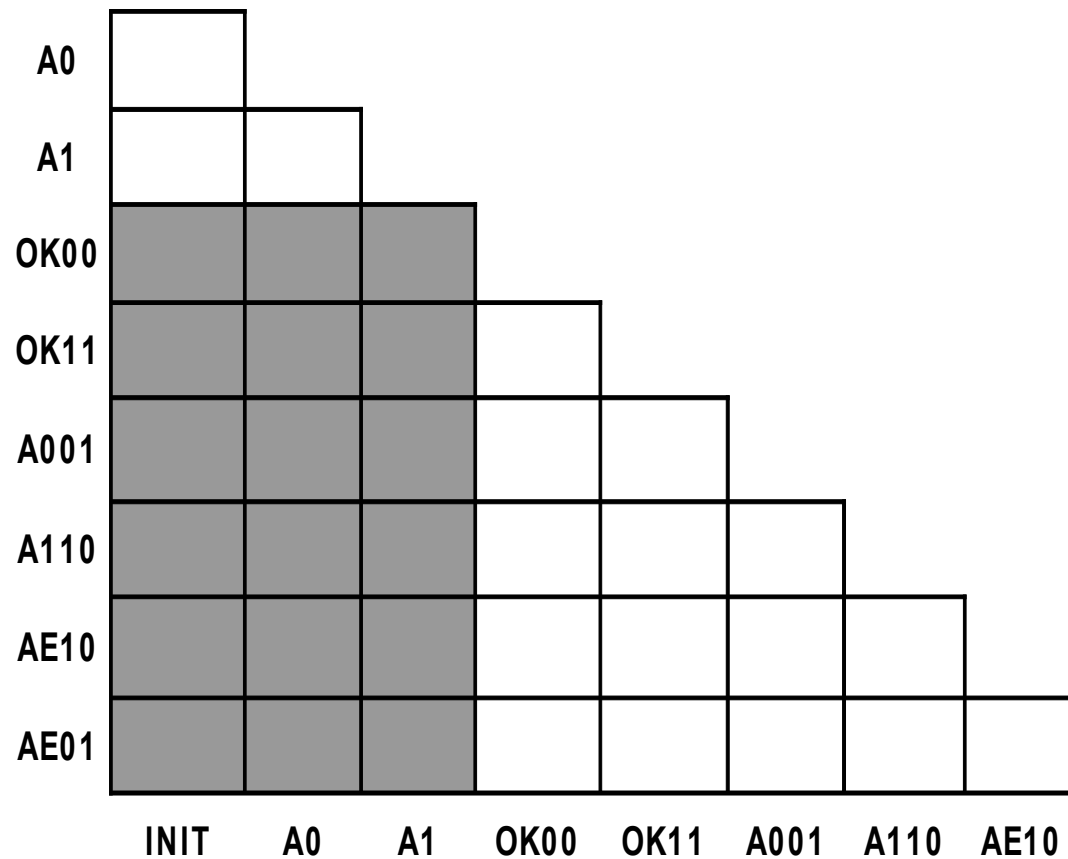


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Digital Design Principles and Practices, 3/e

State Minimization (Nonminimal state table)

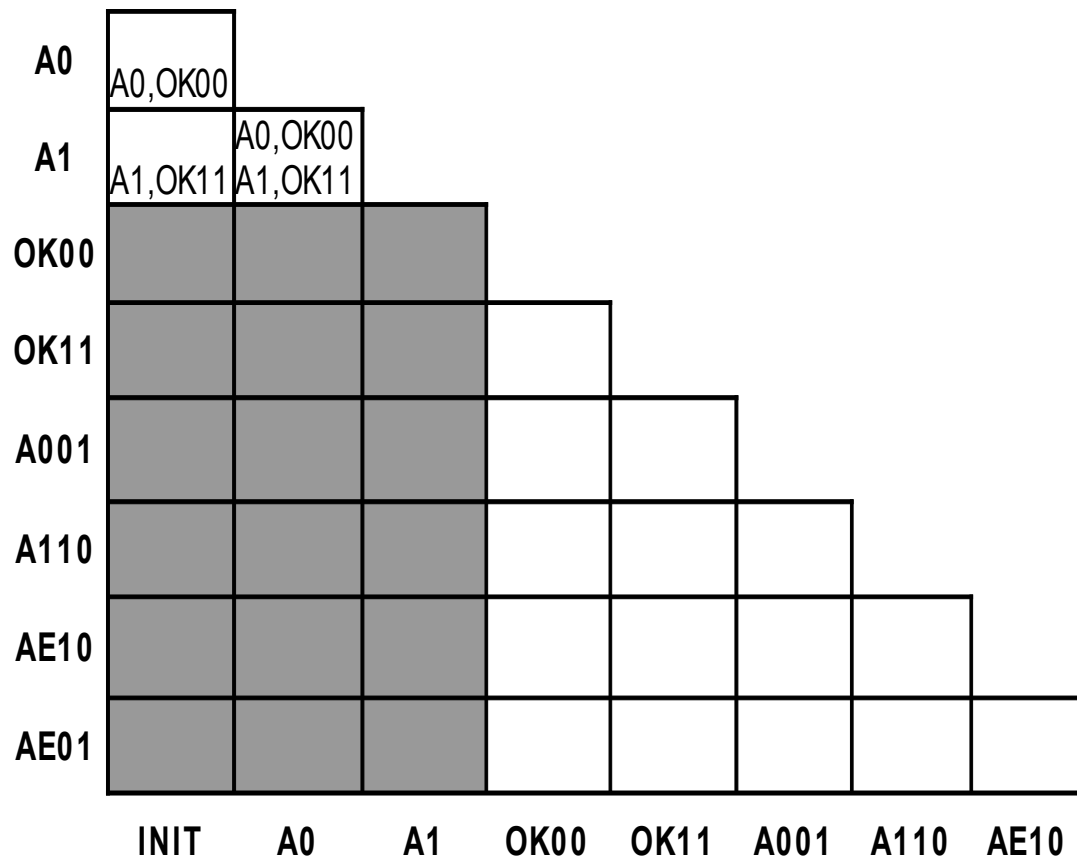
Meaning	AB					
	S	00	01	11	10	Z
Init State	INIT	A0	A0	A1	A1	0
Got 0 on A	A0	OK00	OK00	A1	A1	0
Got 1 on A	A1	A0	A0	OK11	OK11	0
Got 00 on A	OK00	OK00	OK00	A001	A1	1
Got 11 on A	OK11	A0	A110	OK11	OK11	1
Got 001 on A, B=1	A001	A0	AE10	OK11	OK11	1
Got 110 on A, B=1	A110	OK00	OK00	AE01	A1	1
Got bb..10 on A, B=1	AE10	OK00	OK00	AE01	A1	1
Got bb..01 on A, B=1	AE01	A0	AE10	OK11	OK11	1

Implication Chart (Exclude states – output not equal)



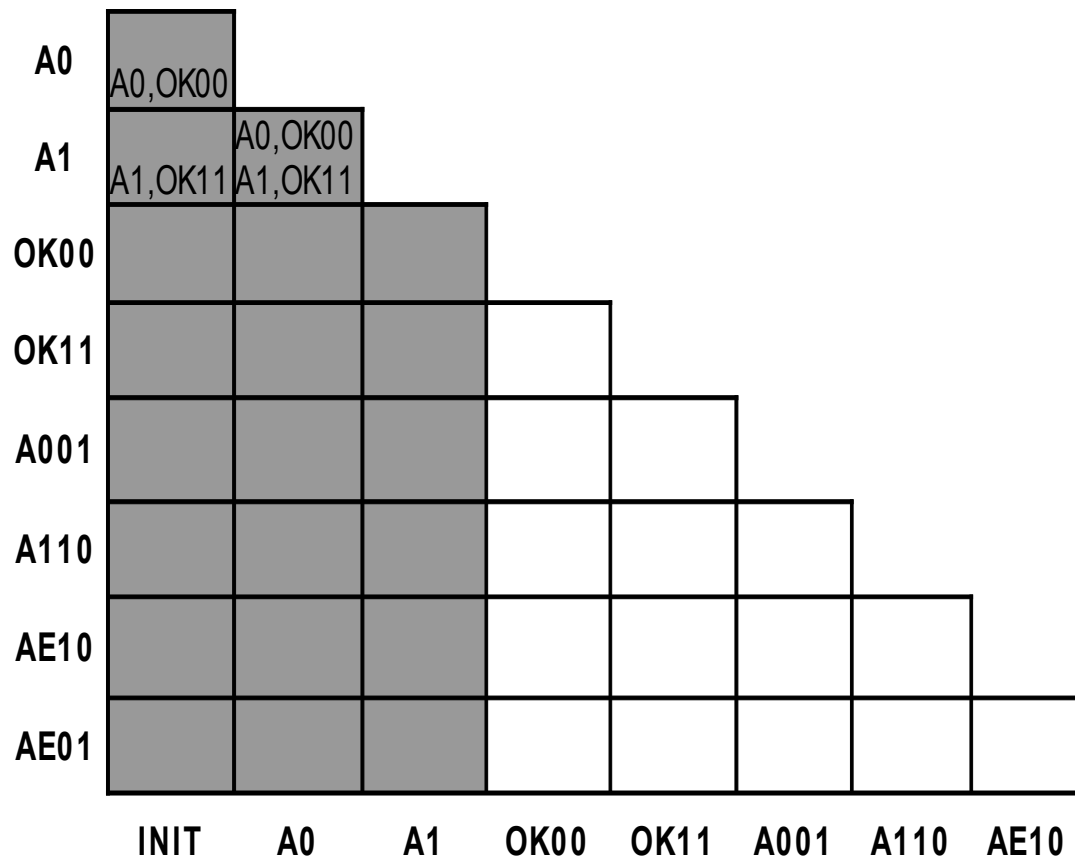
		AB				
S		00	01	11	10	Z
INIT		A0	A0	A1	A1	0
A0		OK00	OK00	A1	A1	0
A1		A0	A0	OK11	OK11	0
OK00		OK00	OK00	A001	A1	1
OK11		A0	A110	OK11	OK11	1
A001		A0	AE10	OK11	OK11	1
A110		OK00	OK00	AE01	A1	1
AE10		OK00	OK00	AE01	A1	1
AE01		A0	AE10	OK11	OK11	1

Implication Chart (First three states)



		AB				
S		00	01	11	10	Z
INIT		A0	A0	A1	A1	0
A0		OK00	OK00	A1	A1	0
A1		A0	A0	OK11	OK11	0
OK00		OK00	OK00	A001	A1	1
OK11		A0	A110	OK11	OK11	1
A001		A0	AE10	OK11	OK11	1
A110		OK00	OK00	AE01	A1	1
AE10		OK00	OK00	AE01	A1	1
AE01		A0	AE10	OK11	OK11	1

Implication Chart (First three states not equal)



S	AB				
	00	01	11	10	Z
INIT	A0	A0	A1	A1	0
A0	OK00	OK00	A1	A1	0
A1	A0	A0	OK11	OK11	0
OK00	OK00	OK00	A001	A1	1
OK11	A0	A110	OK11	OK11	1
A001	A0	AE10	OK11	OK11	1
A110	OK00	OK00	AE01	A1	1
AE10	OK00	OK00	AE01	A1	1
AE01	A0	AE10	OK11	OK11	1

Implication Chart

A0	A0,OK00							
A1	A1,OK11	A0,OK00						
OK00								
OK11			A0,OK00					
A001			A0,OK00	A110,AE10				
A110			A001,AE01	A0,OK00	A0,OK00			
AE10			A001,AE01	A0,OK00	A0,OK00			
AE01			A0,OK00	A110,AE10		A0,OK00	A0,OK00	
	INIT	A0	A1	OK00	OK11	A001	A110	AE10

		AB					
		S	00	01	11	10	Z
INIT		A0	A0	A1	A1		0
A0		OK00	OK00	A1	A1		0
A1		A0	A0	OK11	OK11		0
OK00		OK00	OK00	A001	A1		1
OK11		A0	A110	OK11	OK11		1
A001		A0	AE10	OK11	OK11		1
A110		OK00	OK00	AE01	A1		1
AE10		OK00	OK00	AE01	A1		1
AE01		A0	AE10	OK11	OK11		1

Implication Chart (Reduced to 5 states)

A0	A0,OK00							
A1	A1,OK11	A0,OK00						
OK00								
OK11				A0,OK00				
A001				A0,OK00	A110,AE10			
A110				A001,AE01	A0,OK00	A0,OK00		
AE10				A001,AE01	A0,OK00	A0,OK00		
AE01				A0,OK00	A110,AE10		A0,OK00	A0,OK00
	INIT	A0	A1	OK00	OK11	A001	A110	AE10

S	AB				
	00	01	11	10	Z
INIT	A0	A0	A1	A1	0
A0	OK00	OK00	A1	A1	0
A1	A0	A0	OK11	OK11	0
OK00	OK00	OK00	A001	A1	1
OK11	A0	A110	OK11	OK11	1
A001	A0	AE10	OK11	OK11	1
A110	OK00	OK00	AE01	A1	1
AE10	OK00	OK00	AE01	A1	1
AE01	A0	AE10	OK11	OK11	1

$\left. \begin{array}{l} AE10 = A110 \\ AE01 = A001 \end{array} \right\} \Rightarrow$
 $\left. \begin{array}{l} AE10 = A110 = OK00 = OK0 \\ AE01 = A001 = OK11 = OK1 \end{array} \right\} \Rightarrow$
 States: INIT
 A0
 A1
 OK0
 OK1

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1. Construct state/output table or state diagram.
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3. State assignment – binary code for each state.
4. Create transition/output table – decide how to handle unused states.
5. Select flip-flop type, i.e., D, T or J-K.
6. Construct excitation table.
7. Derive excitation & output equations.
8. Realize logic network with discrete gates & flip-flops or with programmable logic device.

Possible state assignments

State Name	Assignment			
	Simplest Q1-Q3	Decomposed Q1-Q3	One-Hot Q1-Q5	Almost One-Hot Q1-A4
INIT	000	000	00001	0000
A0	001	100	00010	0001
A1	010	101	00100	0010
OK0	011	110	01000	0100
OK1	100	111	10000	1000

Transition and Output Table for Example

Q1	Q2	Q3	AB				Z
			00	01	11	10	
000			100	100	101	101	0
100			110	110	101	101	0
101			100	100	111	111	0
110			110	110	111	101	1
111			100	110	111	111	1

Transition and Output Table for Example

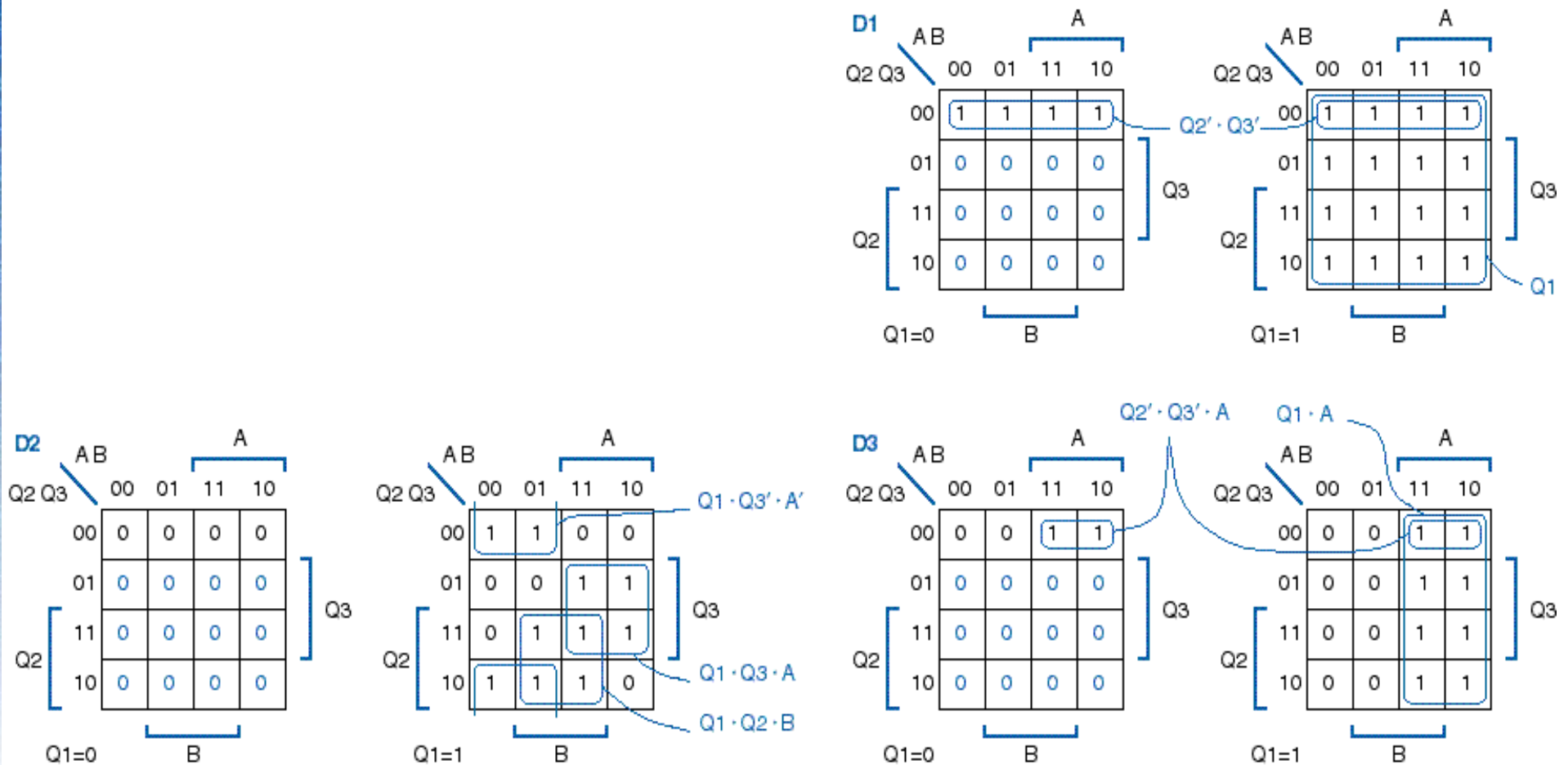
Q1	Q2	Q3	AB				Z
			00	01	11	10	
000			100	100	101	101	0
100			110	110	101	101	0
101			100	100	111	111	0
110			110	110	111	101	1
111			100	110	111	111	1

D1 D2 D3

Excitation K-maps

- Select unused states to be 000, i.e., INIT state

Excitation K-maps for D Flip-Flop



Minimal Risk vs Minimal Cost

- Minimal Risk – unused states set to 000
 - $D1 = Q1 + Q2' \cdot Q3'$
 - $D2 = Q1 \cdot Q3' \cdot A' + Q1 \cdot Q3 \cdot A + Q1 \cdot Q2 \cdot B$
 - $D3 = Q1 \cdot A + Q2' \cdot Q3' \cdot A$
 - $Z = Q1 \cdot Q2$
- Minimal Cost – unused states set to “don't care”
 - $D1 = 1$
 - $D2 = Q1 \cdot Q3' \cdot A' + Q3 \cdot A + Q2 \cdot B$
 - $D3 = A$