

## ELEG 2134: Digital Logic Design – Information & Class Policies

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Office Hours: 10:00am – 12:00pm MWF

9:00am – 11:00am TR

Lecture: 11:00am – 12:20pm TR, COR 114

Text: Wakerly, J.F., *Digital Design Principles & Practices*, 4<sup>th</sup>, Pearson Prentice Hall, 2005. (ISE Student Edition CD not required)

Grade Weighting:	Homework:	5%
	Quizzes:	10%
	Tests (2):	20% (10% each)
	Midterm Exam:	15%
	Final Exam:	30%
	Labs:	20%

Grading Scale:	A: 90% - 100%
	B: 80% - 89%
	C: 70% - 79%
	D: 60% - 69%
	F: < 60%

Class Policies: Students are expected to attend every class. Three or more unexcused absences are grounds for dismissal with a failing grade. Cheating on a quiz or test will result in a zero for that test. Calculators can not be used during exams. The university policies on plagiarism and student misconduct will be strictly enforced. Unless otherwise noted, students may not collaborate on work inside or outside class. Late homework will be accepted; however, points will be deducted for each class period past due date. Students must be co-registered in ELEG 2130.

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### Course Schedule:

- Week 1: Digital concepts and number systems.
- Week 2: Number system conversions, binary codes, binary arithmetic.
- Week 3: Digital Circuits & logic families.
- Week 4: **Test 1.** Introduction to combinatorial logic.
- Week 5: Minimization of logic functions.
- Week 6: Design of combinatorial logic circuits and static hazards.
- Week 7: Introduction to VHDL
- Week 8: **Midterm Exam.** Digital address, subtractors and multipliers.
- Week 9: Flip-Flops, counters and registers.
- Week 10: Introduction to sequential circuits, state machine notation.
- Week 11: Design of synchronous sequential circuits.
- Week 12: Design of synchronous sequential circuits (continued).
- Week 13: Counter design.
- Week 14: Programmable logic devices (CPLD and FPGA).
- Week 15: Memory devices.
- Week 16: **Test 2.** Review