

ELEG 2130 – Digital Logic Design Laboratory Syllabus

2008 - 2009 Catalog Data:	ELEG 2130 – Digital Logic Design Laboratory. Co-requisite: ELEG 2134 (Digital Logic Design). A study of basic digital logic circuit design and implementation. Circuit schematic development utilizing computerized automated design tools. Computer modeling and simulation of digital systems. Emphasis will be placed on proper laboratory techniques, including data collection, data reduction, and report preparation. Laboratory three hours.
Textbook:	J. F. Wakerly, <i>Digital Design: Principles and Practices</i> , 4 th edition, Pearson Prentice Hall, 2005.
Reference:	<ol style="list-style-type: none">1. Texas Instruments Parts Search [http://www-s.ti.com/sc/docs/psheets/pids2.htm]2. Digital Design: Principles & Practices [http://www.ddpp.com/]3. Lab Handouts.
Coordinator:	Carl Greco, Ph.D., Associate Professor of Electrical Engineering
Objectives:	<ol style="list-style-type: none">1. Understanding Boolean algebra and mastery of number systems including binary, hexadecimal and octal. [1]¹2. Development of combinatorial and sequential logic design techniques at the gate and medium-scale integration (MSI) level. [1,3]3. Introduce the student to digital electronic hardware design at the medium and large scale integrated circuit level using VHDL or VHSIC Hardware Description Language where VHSIC is Very High Speed Integrated Circuit. [1, 3]4. Preparation of formal written lab reports. [1,2,3]
Prerequisites by Topic:	<ol style="list-style-type: none">1. Familiarity with the use of computers.2. Sufficient acumen to apply techniques acquired in lecture toward the design of combinatorial and sequential circuits.
Topics:	<ol style="list-style-type: none">1. Binary number and codes.2. Boolean algebra and switching algebra.3. Digital circuits and logic families.4. Combinatorial logic design.5. Sequential logic including state machine design.6. Introduction to VHDL
Laboratory and Computer Projects:	Weekly 3 hour lab covering the following topics: Binary and BCD Counting; Configure a 4-bit binary counter with LED output; Combinational circuit design and minimization; Decoders, multiplexers and encoders; VHDL circuit design and simulation; seven segment LED driver; S-R latch; design a 4-bit counter from J-K flip-flops.
Evaluation Methods:	<ol style="list-style-type: none">A. Participation and notebook (25%)B. Formal Lab Reports (75%)

¹ Refers to the number of the educational objective(s) of the program leading to the BSEE degree at Arkansas Tech University that applies to course objective.

Performance Criteria:

Objective 1:

1. Students will demonstrate an understanding of the binary number system and codes. [A, B]²
2. Students will demonstrate an understanding of Boolean algebra and its applications to digital logic design. [A, B]

Objective 2:

1. Students will demonstrate an understanding of digital circuit and logic families. [A, B]

Objective 3:

1. Students will demonstrate an understanding of combinatorial circuit design and minimization. [A, B]

Objective 4:

Students will demonstrate an understanding of the design, analysis and application of finite-state-machines in sequential circuit. [A, B].

Prepared by:

Carl Greco, Assoc. Prof.

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² Refers to evaluation method(s) to measure student performance.