

## ELEG 2130: Digital Logic Design Lab – Information & Lab Policies

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Office Hours: 10:00am – 12:00pm MWF

9:00am – 11:00am TR

Lab Assistants: TBA

Lab: 3:00 – 6:00 pm, Tuesday, COR 116

Text: 1. Wakerly, J.F., *Digital Design Principles & Practices*, 4<sup>th</sup>, Pearson Prentice Hall, 2005.  
2. Lab handouts.

Grade Weighting<sup>1</sup>: Lab Reports: 75%  
Participation: 25%

Grading Scale: A: 90% - 100%  
B: 80% - 89%  
C: 70% - 79%  
D: 60% - 69%  
F: < 60%

Class Policies: Students are expected to attend every lab. Three or more unexcused absences are grounds for dismissal with a failing grade. If you miss lab for any reason, you must make arrangements with the lab instructor to make it up. Laboratory participation is required. You will be graded on your participation as well as your report. Lab reports are due the week following the completion of the lab. A 10 point reduction in the grade will be applied for each week, or portion thereof, that the report is late. Students may collaborate with their lab partners on the lab work and reports inside and outside lab. Copying or plagiarizing other sources will result in a zero for that report. The university policies on plagiarism and student misconduct will be strictly enforced. Students must be co-registered in ELEG 2134.

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<sup>1</sup> Laboratory grade counts as 20% of the ELEG 2134 course grade.

## **ELEG 2130: Digital Logic Design Lab – Information & Lab Policies**

### Lab Schedule:

- Lab 1: Introduction to lab procedures, Vulcan logic trainer and OrCAD/ Pspice.
- Lab 2: Binary counter.
- Lab 3: Combinational circuit design.
- Lab 4: Parity generator and detector.
- Lab 5: Braille Dot Generator.
- Lab 6: Seven segment decoders and display.
- Lab 7: Combinational circuit implementation with decoders and multiplexers.
- Lab 8: Introduction to VHDL
- Lab 9: Binary adders and comparators.
- Lab 10: S-R latch.
- Lab 11: Binary counter.
- Lab 12: Sequential state machine.